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REMARKS

The above Amendments and these Remarks are being submitted in response to the Office Action dated February 13, 2002.

I. Summary of the Examiner's Rejections

Claims 2-37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fujimoto (U.S. Patent No. 5,912,710).

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II. Summary of the Applicant's Amendments

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The specification has been amended to correct minor grammatical and typographical errors present therein, and to make the specification conform to the originally filed drawings. The Applicant submits that no new matter has been added by such amendments.

III. Applicant's Response to the Examiner's Rejections

The Applicants traverse the rejections of the aforementioned claims for the reasons set forth below.

A. Rejection of Claims 2-19

The instant invention is directed to a method and apparatus for providing independent video and graphics scaling within a video graphics system. As defined in claim 1, the video graphics display engine of the present invention includes, among other things:

"...a single memory operably coupled to the graphics scaler and to the video scaler, the single memory further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block..."

Such an element is not disclosed, taught or suggested in Fujimoto. Accordingly, Fujimoto does not render the invention as defined in claim 4 obvious. As understood, Fujimoto is directed to an image display control apparatus (300) which converts data stored on an independent medium (DVD 100) for presentation in a suitable display format. As disclosed, for example, at col. 5, lines 15-26, the image display control apparatus includes the several components that are used to read data from the DVD medium 100 and provide the read information to a suitable display (200). The image display control apparatus is disclosed as having a VRAM (103) for storing only graphics information read directly from the DVD 100, *see*, for example, col. 5, lines 32-34.

However, as clearly shown, for example, in FIG. 1 and disclosed at col. 6, lines 60-62, the VRAM is not coupled to the video data processing components of the image display control apparatus. Nor is the VRAM used in conjunction with the video data at all (*see*, col. 5, lines 32-34 "...the graphics data are written into the memory..."). Thus, as the VRAM is used to store only graphics data and is clearly not coupled to or used in conjunction with the video data processing components of the image display control apparatus, Fujimoto does not teach or suggest "...a single memory operably coupled to the graphics scaler and to the video scaler..." as defined in claim 4.

Moreover, as the VRAM of Fujimoto does not store video data, it is not possible that the "...stream of video data is fetched from the first memory block..." as defined in claim 4. Consequently, as Fujimoto does not teach or suggest a display engine having at least the aforementioned limitations as defined in claim 4, Fujimoto cannot and does not render the invention as defined in claim 4 obvious.

On page 3 of the instant Office Action, the Examiner has characterized the claimed memory element as being equivalent to "...a first memory (FIG. 1 "100G") having graphics data and a second memory (FIG. 1 "100B") having video data and the two memories coupled to their respective scalars (FIG. 1)." However, this characterization is incongruous to the express disclosure provided in Fujimoto, wherein the components labeled 100G and 100B are those portions provided on a DVD 100 medium, which is separate and independent from the disclosed image display control apparatus, and moreover not a memory. As discussed in greater detail above, Fujimoto is directed to the image display control apparatus, which is defined as element 300, for example, in FIG. 1. As clearly illustrated in FIG. 1 and described throughout the Fujimoto reference, the DVD medium 100 is disclosed as being independent of and external to the image display control apparatus. Thus, the Examiner's characterization of the DVD medium 100 is improper and inaccurate. Consequently, even with the Examiner's improper characterization of the DVD, by its being external to the disclosed image display control apparatus, "...a single memory operably coupled to the graphics scaler and the video scaler..." is still not taught or suggested by Fujimoto as the DVD medium 100 is not part of the image display control apparatus.

Accordingly, as the Examiner's characterization of the reference does not teach or suggest the invention as defined in claim 4; nor does the Fujimoto reference itself disclose the

invention as defined in claim 4, the Applicants respectfully submit that the Fujimoto reference does not teach or suggest the invention as defined in claim 4. Accordingly, reconsideration of the rejection of claim 4 is respectfully requested.

Claims 2-3 and 5-19 directly or indirectly depend upon and include all the limitations of claim 4 and are allowable at least for the reasons set forth above with respect to claim 4. Accordingly, reconsideration of the rejection of claims 2-19 is respectfully requested.

B. Rejection of Claims 20-29

Claim 20 is a method claim which defines the novel way for displaying video graphics data according to the present invention. As defined in claim 20, the method includes the steps of:

“...allocating a first block of a memory for storing the video data stream, the allocating based upon memory needs of the video data stream;
allocating a second block of the memory for storing the graphics data stream,
the allocating based upon memory needs of the graphics data stream...”

Such combination of steps is not disclosed, taught or suggested in Fujimoto. Accordingly, Fujimoto does not render the invention as defined in claim 20 obvious. As discussed in greater detail above in Section III(A), Fujimoto does not disclose a system having a memory coupled to, or operating in conjunction with video data. As disclosed, for example, at col. 5, lines 32-34, Fujimoto discloses a system where VRAM is coupled to and store graphics data only. Fujimoto is silent on the ability to store video data. Moreover, as clearly illustrated in FIG. 1, the VRAM of Fujimoto is not in any way connected to or used for storing video data information. Thus, as Fujimoto does not store video data information, Fujimoto cannot and does not teach or suggest “...allocating a first block of memory for storing the video data stream...” as defined in claim 1.

In addition, Fujimoto does not disclose “...allocating a first block of memory for storing the video data based upon memory needs of a video stream...” or “...allocating a second block of the memory for storing the graphics stream, the allocating based upon memory needs of the graphics data stream...” as the video data is not stored within the image display control apparatus. As defined in claim 20, the video display device of the present invention is capable of allocating portions of the memory based upon memory needs of the larger graphics data system. Such functionality is not taught or suggested in Fujimoto as the graphics and video data is read directly from a DVD medium, which has a fixed amount of memory which cannot be altered or

independently allocated in any fashion by the image display control apparatus. Accordingly, as the DVD medium, is not part of the disclosed image display control apparatus as discussed in greater detail above in Section III(A), nor can the size of the memory on the DVD medium be allocated or adjusted in any way by the image display control apparatus of Fujimoto, Fujimoto cannot and does not teach or suggest a system that performs the following operating steps:

“...allocating a first block of a memory for storing the video data stream, the allocating based upon memory needs of the video data stream...”

and

“...allocating a second block of the memory for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream...”

as defined in claim 20. Consequently, Fujimoto does not render the invention as defined in claim 20 obvious. Accordingly, reconsideration of the rejection of claim 20 is respectfully requested.

Claims 21-29 directly or indirectly depend upon and include all the limitations of claim 20 and are allowable at least for the reasons set forth above with respect to claim 20. Accordingly, reconsideration of the rejection of claims 20-29 is respectfully requested.

C. Rejection of Claim 30

Claim 30 is an apparatus claim which defines a video graphics integrated circuit including, among other things:

“...a frame buffer having memory, wherein the video graphics integrated circuit allocates memory between video data and graphics data based upon memory needs of the video data and the graphics data;
a video scaler operably coupled to the frame buffer, wherein the video scaler scales the video data to produce a scaled data stream...”

Such structural elements are not taught or suggested, or otherwise disclosed in Fujimoto. Consequently, Fujimoto does not render the invention as defined in claim 30 obvious. As discussed in greater detail above, Fujimoto is directed to an image display control apparatus having a structure where video data information is not stored within a single memory. Moreover, Fujimoto does not disclose a memory (i.e. frame buffer) being coupled to or storing video data. As disclosed in Fujimoto, the image display control apparatus includes a VRAM for storing graphics data only (*see*, for example, col. 5, lines 32-34); however, the disclosed VRAM is not coupled to, nor operably interconnected with those portions of the image display control apparatus that perform video data processing. Accordingly, as Fujimoto does not disclose a

video graphics display system at least including the aforementioned limitations, the Applicant respectfully submits that Fujimoto does not render the invention as defined in claim 30 obvious. Accordingly, reconsideration of the rejection of claim 30 is respectfully requested.

D. Rejection of Claims 31-37

Claim 31 is an apparatus claim which defines a video graphics circuit including, among other things:

“...a plurality of memory blocks, wherein each of the plurality of memory blocks stores at least one of video data and graphics data;

a plurality of video scalers, wherein each of the plurality of video scalers is coupled to at least one of the plurality of memory blocks, wherein each video scaler of the plurality of video scalers independently scales at least a portion of the video data to produce a scaled video data stream of a plurality of scaled video data streams independent from the other scaled video data streams of the plurality of scaled video data streams;

a plurality of graphics scalers, wherein each of the plurality of graphics scalers is coupled to at least one of the plurality of memory blocks, wherein each graphics scaler of the plurality of graphics scalers independently scales at least a portion of the graphics data to produce a scaled graphics data stream of a plurality of scaled graphics data stream independent from the other scaled graphics data stream of the plurality of scaled graphics data streams...”

Such combination of structural elements is not taught or suggested in Fujimoto. As discussed in greater detail above, Fujimoto does not disclose the use of a “...plurality of memory blocks...” within the image display control apparatus. On page 7, the Examiner provides a characterization of what comprises the memory blocks (FIG. 1 “100B & 100G”), which as discussed above is being directed to an external and independent DVD medium 100, which does not comprise a component of the disclosed image display control apparatus. Thus, by providing a characterization that is both incongruous to the express disclosure of Fujimoto and still does not provide the structure as defined in claim 31, the Applicants submit that the “...a plurality of memory blocks...” limitation as defined in claim 31 is not taught or suggested by Fujimoto.

In addition, the limitations directed to the “...plurality of video scalers...” and “...plurality of graphics scalers...” is also not taught or suggested in Fujimoto. The Examiner has even indicated that such limitations are not disclosed in Fujimoto on page 7 of the Office Action which states in relevant part “...Fujimoto...fails to disclose a plurality of video scalers and graphics scalers that scale[s] a portion of its respective data independent from the other

plurality of respective data streams..." Thus, as the "...plurality of memory blocks..." limitation is not taught or suggested by Fujimoto, and the Examiner expressly admits that the "...video scalers..." and "...graphics scalers..." limitations of claim 31 are not taught or suggested by Fujimoto, Fujimoto cannot and does not render the invention as defined in claim 31 obvious. Accordingly, reconsideration of the rejection of claim 31 is respectfully requested.

Claims 32-37 directly or indirectly depend upon and include all the limitations of claim 31 and are allowable at least for the reasons set forth above with respect to claim 31. Accordingly, reconsideration of the rejection of claims 31-37 is respectfully requested.

Based on the above amendments and remarks, the Applicant submits that claims 2-37 are now in proper condition for allowance and such action is earnestly solicited.

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0441 for any payment in connection with this communication, including any fees for extension of time, which may be required. The Examiner is invited to call the undersigned if such action might expedite the prosecution of this application.

Respectfully submitted,

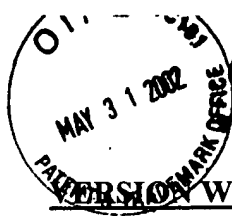
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IN THE SPECIFICATION

Please replace the paragraph beginning on page 9, line 16 with the following:

In other embodiments, there may be a need to display the video information alone or the graphics information alone. In such instances, the system may be equipped with display drivers 166 and/or 176: The display driver 166 receives the scaled video stream 164 from the video scaler 160 and produces a video display signal 168 for display. Similarly, the display driver 176 receives the scaled graphics [scream] stream 174 and produces graphics display signal 178. The display drivers 166 and 176 may be capable of providing an analog output, a digital output, or both.